SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims priority from Korean Patent Application No. 10-2015-0143541, filed on Oct. 14, 2015 in the Korean Intellectual Property Office, and all the benefits accruing therefrom under 35 U.S.C. §119, the contents of which in its entirety are herein incorporated by reference.

BACKGROUND

[0002] 1. Technical Field

[0003] The present disclosure relates to semiconductor devices and/or methods for fabricating the same.

[0004] 2. Description of the Related Art

[0005] For semiconductor device density enhancement, the multigate transistor has been suggested as one of the scaling technologies. In the multigate transistor, a multi-channel active pattern (or silicon body) in a fin or nanowire shape is formed on a substrate and gates are formed on a surface of the multi-channel active pattern.

[0006] Such multigate transistor allows relatively easy scaling because it uses a three-dimensional channel. Further, such multigate transistor tends to have an enhanced current control capability without increasing the gate length of the multigate transistor. Thus, short channel effect (SCE), which is the phenomenon that the electric potential of the channel region is influenced by the drain voltage, can be effectively suppressed.

SUMMARY

[0007] Some example example embodiments of the present disclosure provide semiconductor devices capable of adjusting profiles of a gate electrode and/or a gate spacer by implanting or doping an element semiconductor material into an interlayer insulating layer.

[0008] Some example example embodiments of the present disclosure provide methods for fabricating a semiconductor device capable of adjusting profiles of a gate electrode and/or a gate spacer by implanting or doping an element semiconductor material into an interlayer insulating layer.

[0009] Example example embodiments of the present disclosure are not limited to the example example embodiments mentioned herein, and example example embodiments that are not mentioned herein can be clearly understood to those skilled in the art based on the description provided below.

[0010] According to an example example embodiment of the present inventive concepts, a semiconductor device includes a gate spacer on a substrate, the gate spacer defining a trench, a gate electrode filling the trench, and an interlayer insulating layer on the substrate, which surrounds the gate spacer, the interlayer insulating layer including a first portion having germanium.

[0011] In some example embodiments of the present inventive concepts, a width of the trench may be substantially same with increasing distance from the substrate.

[0012] In some example embodiments of the present inventive concepts, a width of the trench may decrease with increasing distance from the substrate.

[0013] In some example embodiments of the present inventive concepts, the gate electrode may include a first sidewall and a second sidewall opposed to each other, and the first sidewall of the gate electrode and the second sidewall of the gate electrode may have slopes at an acute angle with a bottom surface of the gate electrode.

[0014] In some example embodiments of the present inventive concepts, the gate electrode may include a first sidewall and a second sidewall opposed to each other, the first sidewall of the gate electrode may have a slope at a right angle with a bottom surface of the gate electrode, and the second sidewall of the gate electrode may have a slope at an acute angle with the bottom surface of the gate electrode.

[0015] In some example embodiments of the present inventive concepts, the interlayer insulating layer may include a second portion, which does not include the germanium.

[0016] In some example embodiments of the present inventive concepts, the interlayer insulating layer may include a lower portion and an upper portion, the upper portion of the interlayer insulating layer may include the first portion of the interlayer insulating layer, and the lower portion of the interlayer insulating layer may include the second portion of the interlayer insulating layer, the second portion not including the germanium.

[0017] In some example embodiments of the present inventive concepts, a concentration of the germanium in the first portion of the interlayer insulating layer may increase with increasing distance from the substrate.

[0018] In some example embodiments of the present inventive concepts, an upper surface of the interlayer insulating layer and the upper surface of the gate electrode may be positioned at a same plane.

[0019] In some example embodiments of the present inventive concepts, the semiconductor device may further comprise a fin-type pattern protruding from the substrate. The gate electrode may be on the fin-type pattern and intersects the fin-type pattern.

[0020] In some example embodiments of the present inventive concepts, the semiconductor device may further comprise a source/drain region on the substrate, the source/drain region being adjacent to the gate electrode, and an etch-stop layer extending along respective sidewalls of the gate spacer and an upper surface of the source/drain region.

[0021] In some example embodiments of the present inventive concepts, the interlayer insulating layer may be a single layer.

[0022] According to an example embodiment of the present inventive concepts, a semiconductor device includes a substrate including a first region and a second region, a first gate spacer on the first region, the first gate spacer defining a first trench, a second gate spacer on the second region, the second gate spacer defining a second trench, a first gate electrode filling the first trench, a second gate electrode filling the second trench, a first interlayer insulating layer on the substrate, which surrounds the first gate spacer, and a second interlayer insulating layer on the substrate, which surrounds the second gate spacer. At least one of the first interlayer insulating layer or the second interlayer insulating layer may include germanium.

[0023] In some example embodiments of the present inventive concepts, the first interlayer insulating layer may include the germanium, and the second interlayer insulating layer may not include the germanium.